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POSTER

## **MARU: An ML-Based Framework for Area Estimation from FPGA Resource Usage**

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# MARU: An ML-Based Framework for Area Estimation from FPGA Resource Usage

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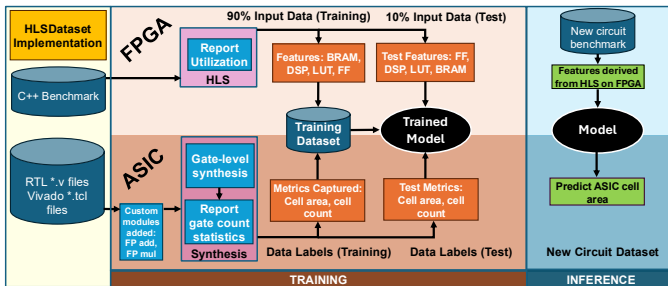


Figure 1: MARU training and inference frameworks using Vitis HLS for FPGA and Yosys for ASIC gate-level synthesis implementations.

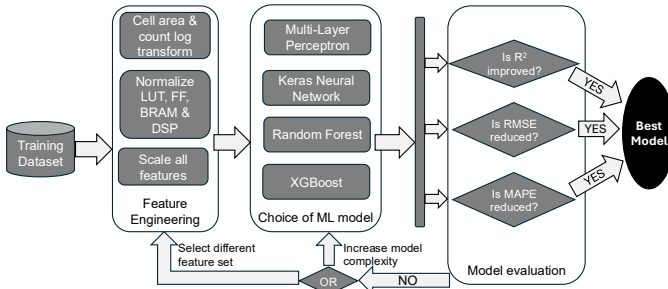


Figure 2: Feature engineering, model choice and evaluation metrics used in MARU learning framework.

## Abstract

FPGA design evaluation faces significant challenges due to heterogeneous resource reporting across vendors and architectures, which hinders performance comparisons and complicates design space exploration. We present MARU (Machine-learning for Area estimation from Resource Usage), a framework that enables FPGA and ASIC area estimation directly from HLS utilization reports.

MARU achieves a mean absolute percentage error of 1.5% and an  $R^2$  of 0.997 in cross-FPGA, multi-circuit predictions, while reducing estimation time from 2.5 days to just 5 minutes per design. The framework enables three key advancements: 1) unified, area-based estimation across diverse FPGA designs, 2) accelerated HLS design space exploration through real-time prediction, and 3) ASIC migration analysis by estimating equivalent area for predictive cost modeling. MARU bridges the FPGA/ASIC methodology gap by providing both a comparative framework for academic research and a practical tool for industry-scale co-design decisions—whether optimizing FPGA implementations or evaluating ASIC transition feasibility through predictive area modeling.

## CCS Concepts

- Computer systems organization → Reconfigurable computing;
- Computing methodologies → Machine learning;
- Hardware → Electronic design automation.

## Keywords

Area Estimation, Application Specific Integrated Circuits

## ACM Reference Format:

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