A NOVEL LOW POWER ENERGY RECOVERY FULL ADDER CELL

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Abstract

A novel low power and low transistor count static energy recovery full adder (SERF) is presented in this paper. The power consumption and general characteristics of the SERF adder are then compared against three low power full adders; the transmission function adder (TFA), the dual value logic (DVL) adder and the fourteen transistor (14T) full adder. The proposed SERF adder design was proven to be superior to the other three designs in power dissipation and area, and second in propagation delay only to the DVL adder. The combination of low power and low transistor count makes the new SERF cell a viable option for low power design.

1. Introduction

The explosive growth in laptop and portable systems and in cellular networks has intensified the research efforts in low power microelectronics. Today there is an ever-increasing number of portable applications requiring low power and high throughput than ever before. For example, notebook and laptop computers, representing the fastest growing segment of the computer industry, are demanding the same computation capabilities as found in desktop machines. Equally demanding are developments in personal communication services (PCS's), such as the current generation of digital cellular telephony networks which employ complex speech compression algorithms and sophisticated radio modems in a pocket sized device. Even more dramatic are the proposed future PCS applications, with universal portable multimedia access supporting full motion digital video and control via speech recognition [1]. Thus, designing low-power digital systems especially the processor is becoming equally important to designing a high performance one.

An adder is one of the most critical components of a processor which determines its throughput, as it is used in the ALU, the floating-point unit, and for address generation in case of cache or memory access. Recently there have been several attempts to design energy recovering logic in the pursuit of energy efficient circuitry [2,3]. Energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. In non-energy recovering logic the charge applied to the load capacitance during logic level high is drained to ground during logic level low. An energy recovering logic reuses charge, which charges the load capacitance during logic high to drive the gates rather than draining charge to ground. Tzartzanis et al [2] recently proposed an energy recovering adder which was shown to be power efficient however it required complex dynamic logic for its operation.

In this paper we present a new low power full adder design, namely the Static Energy-Recovery Full Adder (SERF). The proposed low power energy-recovering logic consumes less energy and has a lower transistor count than previously proposed full adder cells. In order to demonstrate the efficiency of the new design, in this paper, we compare the power consumption and other general characteristics of the SERF design against three other low power full adder cells proposed in past literature [6] [7] [8].

2. Background and Prior Research

The three major components that contribute to the power consumption in CMOS circuits are the static dissipation due to leakage current, the dissipation due to switching transient current and the dissipation due to charging and discharging of load capacitance. The total power in a CMOS circuit is given by the following equation [4]

$$P = \Sigma i\ V_{DD}\ V_{swing}\ C_{load}\ f\ Pi + V_{DD}\ \Sigma i\ I_{isc} + V_{DD}\ I_l$$

where V_{DD} is the power supply voltage, V_{swing} is the voltage swing of the output which is ideally equal to V_{DD}, C_{load} is the output load capacitance at node i, f is the system clock frequency, P_i is the switching activity at node i, I_{isc} is the short circuit current at node i, and I_l is the leakage current. The summation is over all the nodes of the circuit. It is important to note that, in simulation studies, the number of simulation cycles that are needed for accurate estimation of the switched capacitance is critical. It is recommended to have between 50 and 100 simulation cycles for an accurate estimation of the capacitance [5]. A reduction in any of the appropriate components in the above equation will obviously reduce power consumption.

Several designs of low power adder cells can be found in the literature [6] [7] [8]. The transmission function full adder [6], which uses 16 transistors for the realization of the circuit, is shown in Figure 1. For this circuit there are two possible short circuit paths to ground. This design uses both pull-up and pull-down logic as well as complementary pass logic to drive the load. The DVL full adder [7] illustrated in Figure 2, uses 23 transistors for the realization of the adder function. DVL was developed to improve the characteristics of double pass transistor logic which was designed to have the logic level high signal passed to the load through a p-transistor and the logic level low drained from the load through an n-transistor. The fourteen transistor full-adder [8], as the name implies, uses 14 transistors to realize the adder function (See Figure 3). To date this is the most area efficient design. The 14T full adder cell, like the transmission function full adder cell, implements the complementary pass logic to drive the load. The performance of these three adder circuits is compared with the new SERF adder design and the results are given in the following section.

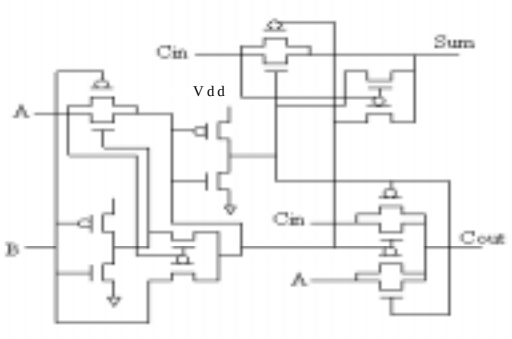

Figure 1. The transmission function adder (TFA) [6]

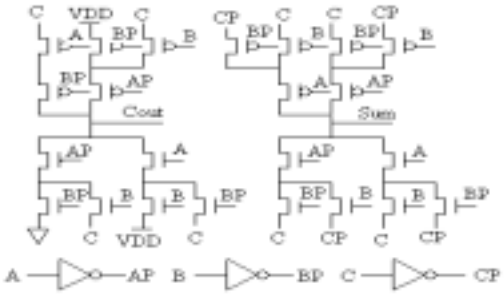

Figure 2. The dual value logic (DVL) adder [7]

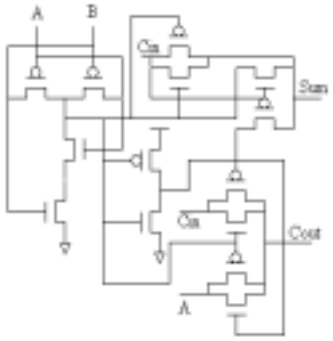

Figure 3. The fourteen transistor (14T) adder [8]

3. Static Energy-Recovery Full Adder

As an initial step toward designing low power arithmetic circuit modules, we designed a Static Energy Recovery Full adder (SERF) cell module illustrated in Figure 4. The cell uses only 10 transistors and it does not need inverted inputs. The design was inspired by the XNOR gate full adder design. In non-energy recovery design the charge applied to the load capacitance during logic level high is drained to ground during the logic level low. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption, removing the Psc variable (product of Isc and voltage) from the total power equation. The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design. To the best of our knowledge this new design has the lowest transistor count for the complete realization of a full adder.

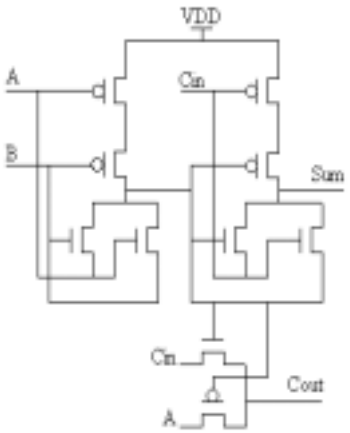

Figure 4. The New Static Energy-Recovery Full (SERF) Adder

The performance of the SERF full adder cell is compared for power consumption, delay and silicon area against the transmission function adder (TFA) [6], dual value logic (DVL) adder [7], and the fourteen transistor (14T) adder [8].

4. Simulation Methodology and Results

Two bit and eight bit ripple carry adders using the previously discussed full adder cells as basic blocks were constructed and modeled in PSPICE using 1.2u and 0.6u transistors. The SERF and the three full adders chosen from the literature (and shown in Figures 1, 2 and 3), were modeled. The simulations were conducted at 50MHz to 200MHz for 300ns while skipping initial transient solution. Buffers were placed between the full adder stages of the ripple carry adders to allow for strong signal propagation. All input and output signals were buffered.

The power consumed by the adders was determined by the following equation [1].

$$P_{total} = \int_{0}^{T} V_{DD} \cdot I_{instantaneous}$$

Where V_{DD} is the supply voltage, $I_{instantaneous}$ is the instantaneous supply current and T is the simulation cycle time. This method of power estimation takes into account static, dynamic and short circuit power dissipation to give a complete and accurate power dissipation analysis for P_{total}.

The results of the simulations for the 2-bit full adders are presented in Table 1. The results show that the SERF cell is far superior in transistor count with only 10 transistors. While transistor count is an inaccurate method for area analysis, transistor count does provide a guideline as to possible die area consumption for the differing design structures. Table 2 illustrates the results for the 8-bit ripple carry adders. A graphical comparison of delay and power are presented in Figures 5 and 6.

Table 1 Delay and Area Comparison Results for 2-bit RCA Analysis

	5V 1.2u	3.3V .6u	
	SUM + COUT	SUM + COUT	
TYPE	DELAY (ns)	DELAY (ns)	TRANSISTOR COUNT
SERF	2.3632	1.6333	10
TFA	2.0000	1.0938	16
DVL	1.0625	0.6667	23
14T	1.5789	0.8615	14

Table 2 Energy Consumption and Delay Comparison Results for the 8-bit RCA Analysis

	5V			3.3V			5V 1.2u	3.3V .6u
	1.2u			.6u			CRIT. DELAY (ns)	CRIT. DELAY (ns)
TYPE	50 MHz (nJ)	100 MHz (nJ)	200 MHz (nJ)	50 MHz (nJ)	100 MHz (nJ)	200 MHz (nJ)		
SERF	0.28	0.43	0.75	0.08	0.12	0.201	5.94	3.39
TFA	0.37	0.75	1.40	0.10	0.20	0.393	8.13	4.83
DVL	0.35	0.85	1.66	0.92	0.21	0.422	5.44	3.26
14T	0.45	0.79	1.25	0.16	0.20	0.358	7.33	4.19

A careful examination of the results shows that the proposed SERF adder design takes approximately 26% to 55% less energy than the other three designs chosen from the literature for error free operation. The DVL adder was the fastest, however it used 23 transistors and 50% more energy than the SERF did. Compared to the 14T adder design, which is the fastest among the remaining adder designs selected for comparison, the SERF design is shown to be 19% faster. Since the new SERF design needs only 10 transistors for the adder circuit realization obviously it is the most area efficient design.

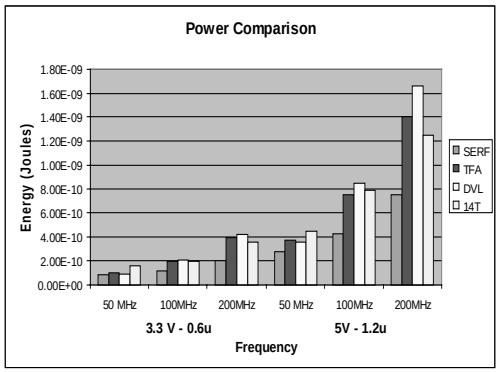

Figure 5. Comparison of Power Consumption of 8-bit SERF Adder to Other Full Adders

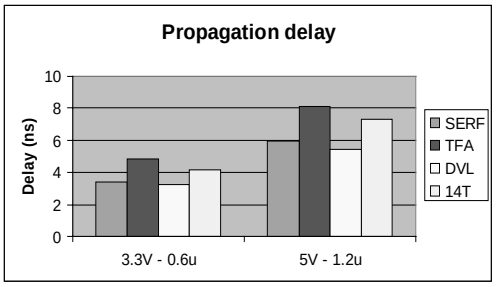

Figure 6. Comparison of Propagation Delay of Various 8-bit Full Adders

5. Conclusion

In this paper we presented a novel low power and low transistor count static energy-recovering full adder and compared its performance against three other full adder cells for power consumption, area and delay. The three full adder cells for comparison against SERF adder were selected recent literature on the topic of low power design. Analysis and simulation studies were performed on 2-bit and 8-bit ripple carry adders. The proposed SERF adder design was proven to be superior to the other three designs in power dissipation and area, and second in propagation delay only to the DVL adder. The combination of low power and low transistor count makes the new SERF adder cell a viable option for low power design.

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* *E. John's research is supported by the National Science Foundation under grant number ECS-9714993. L. John's research is supported by the National Science Foundation under grant numbers CCR-9796098, EIA-9807112, the State of Texas Advanced Technology Program and the University of Texas.*